UNITED STATES PATENT APPLICATION FOR:

APPARATUS, SYSTEM AND METHOD FOR RECEIVER EQUALIZATION

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APPARATUS, SYSTEM AND METHOD FOR RECEIVER EQUALIZATION

RELATED APPLICATION

[0001] This application is related to an application entitled "APPARATUS, AMPLIFIER, SYSTEM AND METHOD FOR RECEIVER EQUALIZATION", inventor Ken DROTTAR, filed on June 27, 2003.

TECHNICAL FIELD

[0002] The inventions generally relate to receiver equalization.

BACKGROUND

[0003] Point-to-point interconnects between two ICs (Integrated Circuits) or ASICs (Application Specific Integrated Circuits) are becoming a widely accepted bus technology for high speed data transfer applications. The signaling scheme for such links can be single-ended or differential. Inter-symbol interference (ISI) due to the interconnect frequency dependent insertion loss characteristics becomes an even larger problem with current printed circuit board (PCB) technology. ISI is one of the primary bottlenecks in implementation of point-to-point high speed interconnection technology.

[0004] Various on-die receiver equalization techniques can be used to reduce the inter-symbol interference (ISI) generated by the frequency dependent loss characteristics of PCB traces. Some known receiver equalization techniques include equalization schemes with a digital filter and equalization schemes with an active linear filter.

[0005] Receiver equalization techniques using a digital filter use an appropriate active digital FIR filter (finite impulse response filter) or an IIR filter (infinite impulse response filter) at the receiver end to cancel out the frequency dependent loss characteristics. One example of such a digital filter is an adaptive-tapped-delay-line-filter implemented at the receiver end. Digital filter receiver equalization techniques at the receiver end are advantageous, but difficult to implement in silicon. Digital filter receiver equalization circuits using FIR or IIR filters dissipate a lot of power. The coefficient of such a digital adaptive filter can be determined using a suitable training sequence and a high order filter scheme is possible, but implementation is extremely complex. It is difficult to obtain gain during implementation of this stage due to limited available voltage headroom.

[0006] Equalization schemes with an active linear filter is easy to implement and circuits using these schemes are able to dissipate power appropriately. Additionally, interconnects with a large loss can be equalized. This can lead to use of longer length interconnects. However, active filters are typically implemented using gm-c circuit elements, which have limited bandwidth.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The inventions will be understood more fully from the detailed description given below and from the accompanying drawings of some embodiments of the inventions which, however, should not be taken to limit the inventions to the specific embodiments described, but are for explanation and understanding only.

[0008] FIG 1 is a circuit representation of an apparatus according to some embodiments of the inventions.

[0009] FIG 2 is a circuit representation of an apparatus according to some embodiments of the inventions.

[0010] FIG 3 is a circuit representation of an apparatus according to some embodiments of the inventions.

[0011] FIG 4 is a block diagram representation of an apparatus according to some embodiments of the inventions.

[0012] FIG 5 is a graphical representation according to some embodiments of the inventions.

[0013] FIG 6 is a block diagram representation of an apparatus according to some embodiments of the inventions.

[0014] FIG 7 is a block diagram representation of an apparatus according to some embodiments of the inventions.

[0015] FIG 8 is a block diagram representation of a system according to some embodiments of the inventions.

DETAILED DESCRIPTION

[0016] Some embodiments of the inventions relate to receiver equalization. In some embodiments adaptive equalization is implemented at a receiver. In some embodiments adaptive equalization is performed for signals transmitted over point-to-point intereconnects (for example, between chips), high speed data buses, or any other high speed serial interconnect.

[0017] In some embodiments, a frequency dependent gain circuit is coupled to an output of an amplifier. The gain circuit provides at least two ranges of frequency dependent gain characteristics in response to the output of the amplifier. A control circuit provides one of the at least two gain values as an output.

[0018] In some embodiments a CMOS (Complementary Metal Oxide Semiconductor) adaptive equalization circuit is used that is based on an RC filter in order to reduce inter-symbol interference (ISI). In some embodiments the equalization circuit and/or the RC filter are

realized using an on-die passive resistance and capacitance elements. In some embodiments adaptive feedback is based on 8B/10B encoded signal characteristics of DC balance (for example, in order to track temperature and process variations). In some embodiments it is possible for a generic high speed receiver to be optimized for given interconnects using digital control elements. In some embodiments a resistance R is realized using passive components (for example, poly resistance, gbn-well, and/or diffused), or with active components (for example, using a pass gate, an n-well pass gate, etc.). In some embodiments a capacitance C is realized using metal-to-metal capacitance, with a pMOS gate to source/drain capacitance or with nMOS gate to source/drain capacitance when nMOS isolated well is available.

[0019] In some embodiments resistance and capacitance values are dependent on insertion loss characteristics of the interconnect and the termination resistance. In some embodiments adaptive equalization is performed to adjust the equalization based on desired interconnect insertion loss characteristics. In order to obtain variable discrete frequency dependent gain, two or more equalization circuits may be cascaded (or attached in series) in some embodiments, where the outputs of the equalization circuits are fed in a multiplexed fashion. In some embodiments discrete gain values are provided. In some embodiments one of a group of two or more discrete gain values are selected as an output value. In some embodiments the selection is performed using DC balance techniques. In some embodiments the selection is performed using 8B/10B encoded signal characteristics of DC balance.

[0020] FIG 1 illustrates an apparatus 100 according to some embodiments. Apparatus 100 includes an input Vin, an inverse input $\overline{EN1}$, an input EN1, an output A*Vin, a p-channel MOSFET 102 (Metal Oxide Semiconductor Field Effect Transistor) (pMOS transistor 102), a pMOS transistor 104, an n-channel MOSFET 106 (nMOS transistor 106), an nMOS transistor 108 and a resistor 110. In some embodiments apparatus 100 is a CMOS amplifier.

In some embodiments apparatus 100 is a high bandwidth low gain CMOS amplifier. In some embodiments apparatus 100 is an equalizer circuit or is a building block for an equalizer circuit.

[0021] A source of pMOS transistor 102 is coupled to a high voltage source Vss. A gate of pMOS transistor 102 is coupled to the inverse input $\overline{EN1}$. A drain of pMOS transistor 102 is coupled to a source of pMOS transistor 104.

[0022] A source of pMOS transistor 104 is coupled to the drain of pMOS transistor 102. A gate of pMOS transistor 104 is coupled to the input Vin, to a first terminal of resistor 110, and to a gate of nMOS transistor 106. A drain of pMOS transistor 104 is coupled to a second terminal of resistor 110, to the output A*Vin, and to a drain of nMOS transistor 106.

[0023] A source of nMOS transistor 106 is coupled to a drain of nMOS transistor 108. A gate of nMOS transistor 106 is coupled to the input Vin, to the first terminal of resistor 110, and to the gate of pMOS transistor 104. A drain of nMOS transistor 106 is coupled to the drain of pMOS transistor 104, to the second terminal of resistor 110 and to the output A*Vin.

[0024] A source of nMOS transistor 108 is coupled to a low level voltage source Vcc. In some embodiments the low level voltage source Vcc is a ground voltage. A gate of nMOS transistor 108 is coupled to the input EN1. A drain of nMOS transistor 108 is coupled to the source of nMOS transistor 106.

[0025] Resistor 110 has a resistance R1. A first terminal of resistor 110 is coupled to the input Vin, the gate of pMOS transistor 104 and the gate of nMOS transistor 106. A second terminal of resistor 110 is coupled to the output A*Vin, the drain of pMOS transistor 104 and the drain of nMOS transistor 106. Resistor 110 is coupled between the input and the output of apparatus 100, which is in some embodiments a modified CMOS amplifier. Resistance R1 of resistor 110 provides negative feedback to the CMOS amplifier 100 and therefore increases the bandwidth of the amplifier, and the circuit becomes self biased. An output

impedance of amplifier 100 is approximately equal to the resistance R1 of resistor 110. An input impedance of amplifier 100 is approximately equal to R1/(1+A), where R1 is the resistance of resistor 100 and A is the gain of the amplifier 100. The voltage gain of amplifier 100 is equal to –A, where A is the gain of the amplfier.

[0026] FIG 2 illustrates an apparatus 200 according to some embodiments. In some embodiments apparatus 200 is an equalization circuit. Apparatus 200 includes an input Vin, an inverse input $\overline{EN1}$, an input EN1, an output Vout, a pMOS transistor 202, a pMOS transistor 204, an nMOS transistor 206, an nMOS transistor 208, a resistor 210, a resistor 212 and a capacitor 214. Transistors 202, 204, 206 and 208 and resistor 210 are similar to transistors 102, 104, 106 and 108 and resistor 110 illustrated in and described in reference to FIG 1, and may be exactly the same as the elements in FIG 1.

[0027] A source of pMOS transistor 202 is coupled to a high voltage source Vss. A gate of pMOS transistor 202 is coupled to the inverse input $\overline{EN1}$. A drain of pMOS transistor 202 is coupled to a source of pMOS transistor 204.

[0028] A source of pMOS transistor 204 is coupled to the drain of pMOS transistor 202. A gate of pMOS transistor 204 is coupled to a first terminal of resistor 210, to a gate of nMOS transistor 206, to a second terminal of resistor 212, and to a second terminal of capacitor 214. A drain of pMOS transistor 204 is coupled to a second terminal of resistor 210, to the output Vout, and to a drain of nMOS transistor 206.

[0029] A source of nMOS transistor 206 is coupled to a drain of nMOS transistor 208. A gate of nMOS transistor 206 is coupled to the first terminal of resistor 210, to the gate of pMOS transistor 204, to the second terminal of resistor 212 and to the second terminal of capacitor 214. A drain of nMOS transistor 206 is coupled to the drain of pMOS transistor 204, to the second terminal of resistor 210 and to the output Vout.

[0030] A source of nMOS transistor 208 is coupled to a low level voltage source Vcc. In some embodiments the low level voltage source Vcc is a ground voltage. A gate of nMOS transistor 208 is coupled to the input EN1. A drain of nMOS transistor 208 is coupled to the source of nMOS transistor 206.

[0031] Resistor 210 has a resistance R1. This resistance R1 of resistor 210 may be the same as or different than the resistance R1 of resistor 110 illustrated in FIG 1. A first terminal of resistor 210 is coupled to a second terminal of resistor 212, to a second terminal of capacitor 214, to the gate of pMOS transistor 204 and to the gate of nMOS transistor 206. A second terminal of resistor 210 is coupled to the output Vout, to the drain of pMOS transistor 204 and to the drain of nMOS transistor 206.

[0032] Resistor 212 has a resistance R2 that may be the same resistance as or a different resistance than resistance R1 of resistor 210. Further, as mentioned above, the resistance R1 of resistor 210 need not be the same value as the resistance R1 of resistor 110 of FIG 1. A first terminal of resistor 212 is coupled to the input Vin and to a first terminal of capacitor 214. A second terminal of resistor 212 is coupled to a second terminal of capacitor 214, a terminal of resistor 210, a gate of pMOS transistor 204 and a gate of nMOS transistor 206.

[0033] Capacitor 214 has a capacitance C1 that may be any value. A first terminal of capacitor 214 is coupled to the input Vin and to a first terminal of resistor 212. A second terminal of capacitor 214 is coupled to a second terminal of resistor 212, a terminal of resistor 210, a gate of pMOS transistor 204 and a gate of nMOS transistor 206.

[0034] In some embodiments the resistor 212 and capacitor 214 are an on die R2 and C1 resistive network. In some embodiments apparatus 200 may be referred to as an equalization circuit with an on die resistive network (including resistor 212 and capacitor 214) followed by a modified CMOS amplifier (including transistors 202, 204, 206 and 208 and resistor 210). In

some embodiments the value of R1, R2 and C1 may be set or fixed to provide a predetermined level of quantified equalization.

[0035] FIG 3 illustrates an apparatus 300 according to some embodiments. In some embodiments FIG 3 is an equalization circuit. In some embodiments apparatus 300 is referred to as an equalization block or a complete equalization block. Apparatus 300 includes an input IN, an inverse input $\overline{EN1}$, an input EN1, an output OUT, a pMOS transistor 302, a pMOS transistor 304, an nMOS transistor 306, an nMOS transistor 308, a resistor 310, a resistor 312, a capacitor 314, a pMOS transistor 322, a pMOS transistor 324, an nMOS transistor 326, an nMOS transistor 328 and a resistor 330 . Transistors 302, 304, 306 and 308 and resistor 310 are similar to transistors 102, 104, 106 and 108 and resistor 110 illustrated in and described in reference to FIG 1 and are similar to transistors 202, 204, 206 and 208 and resistor 210 illustrated in and described in reference to FIG 2, and may be exactly the same as the elements in FIG 1 and/or FIG 2. Similarly resistor 312 and capacitor 314 are similar to resistor 212 and capacitor 214 illustrated in and described in reference to FIG 2, and may be exactly the same as the elements in FIG 2.

[0036] A source of pMOS transistor 302 is coupled to a high voltage source Vss. A gate of pMOS transistor 302 is coupled to the inverse input $\overline{EN1}$. A drain of pMOS transistor 302 is coupled to a source of pMOS transistor 304.

[0037] A source of pMOS transistor 304 is coupled to the drain of pMOS transistor 302. A gate of pMOS transistor 304 is coupled to a first terminal of resistor 310, to a gate of nMOS transistor 306, to a second terminal of resistor 312, and to a second terminal of capacitor 314. A drain of pMOS transistor 304 is coupled to a second terminal of resistor 310, to the output OUT, and to a drain of nMOS transistor 306.

[0038] A source of nMOS transistor 306 is coupled to a drain of nMOS transistor 308. A gate of nMOS transistor 306 is coupled to the first terminal of resistor 310, to the gate of pMOS

transistor 304, to the second terminal of resistor 312 and to the second terminal of capacitor 314. A drain of nMOS transistor 306 is coupled to the drain of pMOS transistor 304, to the second terminal of resistor 310 and to the output OUT.

[0039] A source of nMOS transistor 308 is coupled to a low level voltage source Vcc. In some embodiments the low level voltage source Vcc is a ground voltage. A gate of nMOS transistor 308 is coupled to the input EN1. A drain of nMOS transistor 308 is coupled to the source of nMOS transistor 306.

[0040] Resistor 310 has a resistance R1. This resistance R1 of resistor 310 may be the same as or different than either the resistance R1 of resistor 110 illustrated in FIG 1 or the resistance R1 of resistor 210 illustrated in FIG 2. A first terminal of resistor 310 is coupled to a second terminal of resistor 312, to a second terminal of capacitor 314, to the gate of pMOS transistor 304 and to the gate of nMOS transistor 306. A second terminal of resistor 310 is coupled to the output OUT, to the drain of pMOS transistor 304 and to the drain of nMOS transistor 306.

[0041] Resistor 312 has a resistance R2 which may be the same resistance as or a different resistance than resistance R1 of resistor 310 in FIG 3, resistance R2 of resistor 212 in FIG 2, resistance R1 of resistor 210 in FIG 2, or resistance R1 of resistor 110 in FIG 1. Further, as mentioned above, the resistance R1 of resistor 310 need not be the same value as the resistance R1 of resistor 110 of FIG 1 or the resistance R1 of resistor 210 of FIG 2. A first terminal of resistor 312 is coupled to a drain of pMOS transistor 324, a second terminal of resistor 330, a drain of nMOS transistor 326, and to a first terminal of capacitor 314. A second terminal of resistor 312 is coupled to a second terminal of capacitor 314, to a first terminal of resistor 310, to a gate of pMOS transistor 304 and to a gate of nMOS transistor 306.

[0042] Capacitor 314 has a capacitance C1 which may be any value. Capacitance C1 of capacitor 314 may be the same as or different than the capacitance C1 of capacitor 214 of

FIG 2. A first terminal of capacitor 314 is coupled to a drain of pMOS transistor 324, a second terminal of resistor 330, a drain of nMOS transistor 326, and to a first terminal of resistor 312. A second terminal of capacitor 314 is coupled to a second terminal of resistor 312, to the first terminal of resistor 310, to a gate of pMOS transistor 304 and to a gate of nMOS transistor 306.

[0043] A source of pMOS transistor 322 is coupled to a high voltage source Vss. A gate of pMOS transistor 322 is coupled to the inverse input $\overline{EN1}$. A drain of pMOS transistor 322 is coupled to a source of pMOS transistor 324.

[0044] A source of pMOS transistor 324 is coupled to the drain of pMOS transistor 322. A gate of pMOS transistor 324 is coupled to the input IN, to a first terminal of resistor 330, and to a gate of nMOS transistor 326. A drain of pMOS transistor 324 is coupled to a second terminal of resistor 330, to the first terminal of resistor 312, to the first terminal of capacitor 314, and to a drain of nMOS transistor 326.

[0045] A source of nMOS transistor 326 is coupled to a drain of nMOS transistor 328. A gate of nMOS transistor 326 is coupled to the first terminal of resistor 330, to the gate of pMOS transistor 324, and to the input IN. A drain of nMOS transistor 326 is coupled to the drain of pMOS transistor 302, to the first terminal of resistor 312 and to the first terminal of capacitor 314.

[0046] A source of nMOS transistor 328 is coupled to a low level voltage source Vcc. In some embodiments the low level voltage source Vcc is a ground voltage. A gate of nMOS transistor 328 is coupled to the input EN1. A drain of nMOS transistor 328 is coupled to the source of nMOS transistor 326.

[0047] A first terminal of resistor 330 is coupled to the input IN, to the gate of pMOS transistor 324 and to the gate of nMOS transistor 326. A second terminal of resistor 330 is coupled to the drain of pMOS transistor 324, to the drain of nMOS transistor 326, to the first terminal of

resistor 312, and to the first terminal of capacitor 314. Resistor 330 has a resistance R3 which may be the same resistance as or a different resistance than resistance R2 of resistor 312 in FIG 3, resistance R2 of resistor 212 in FIG 2, resistance R1 of resistor 310 in FIG 3, resistance R1 of resistor 210 in FIG 2, or resistance R1 of resistor 110 in FIG 1. In some embodiments the resistance R3 of resistor 330 is the same as the resistance R1 of resistor 310 in FIG 3.

[0048] In some embodiments the low frequency response of the equalization circuit 300 is dependent on resistance ratios, and is therefore process independent. In some embodiments the shape of the frequency dependent transfer characteristics of the equalization circuit 300 is a function of the capacitance C1 of capacitor 314 times the resistance R2 of resistor 312 (that is a function of C1*R2). In some embodiments of an equalization circuit such as where the shape of frequency dependent characteristics is a function of C1*R2, the characteristics are process and temperature dependent, and it is beneficial to track them with adaptive feedback. The adaptive feedback can depend on the input signal characteristics.

[0049] In some embodiments the resistance and capacitance values such as R2 and C1 are fixed during a design phase such that they are dependent on insertion loss characteristics of the interconnect and the termination resistance. In some embodiments in order to track process variations the resistances R1, R2 and R3 of any of the embodiments illustrated and described herein are formed with the same technology. For example, if resistance R1 of some embodiments of FIG 3 is poly resistance then R2 and R3 should be of poly resistance. Additionally, the resistances and capacitances (for example, R1, R2, R3 and C1) are fixed during circuit design phase and are not varied during circuit operation.

[0050] In some embodiments adaptive equalization is performed to adjust the equalization based on desired interconnect insertion loss characteristics. In order to obtain variable discrete frequency dependent gain, two or more equalization circuits may be cascaded (or attached in

series) in some embodiments, where the outputs of the equalization circuits are fed in a multiplexed fashion.

[0051] FIG 4 illustrates an apparatus 400 according to some embodiments. In some embodiments apparatus 400 is an equalization circuit providing an output OUT equalization value. Apparatus 400 includes an amplifier 402, two or more equalization circuits 404, 406 and 408, two or more inverters 410, 412 and 414 and a multiplexer 416. In some embodiments, amplifier 402, two or more equalization circuits 404, 406 and 408 and two or more inverters 410, 412 and 414 may be referred to as a gain circuit that supplies two or more discrete gain values V#1, V#2,....., V#n.

[0052] Amplifier 402 has two differential inputs IN and $\overline{IN}$ and a single ended output that is provided as an input IN#1 to equalizer circuit 404. In some embodiments amplifier 402 is a CMOS amplifier. In some embodiments amplifier 402 is a high bandwidth low gain CMOS amplifier. In some embodiments amplifier 402 is a wide band differential to single ended amplifier.

[0053] Equalization circuits 404, 406 and 408 may be each be any type of equalization circuit. FIG 4 shows three equalization circuits 404, 406 and 408. However, any number of equalization circuits may be used in different embodiments, as shown by the dotted lines between the output OUT#2 of equalization circuit 406 and the input IN#n of equalization circuit 408. In some embodiments any or all of the two or more equalization circuits (including any specifically not shown in FIG 4) may be implemented using the equalization circuits illustrated in and described in reference to FIG 1, FIG 2 and/or FIG 3. In some embodiments all of the equalization circuits are exactly the same. In some embodiments the equalization circuits are different from each other. In some embodiments some of the equalization circuits are the same and some are different from each other.

[0054] Equalization circuits 404, 406 and 408 are cascaded (coupled in series). Inverters 410, 412 and 414 are respectively coupled to outputs of equalization circuits 404, 406 and 408 to provide discrete gain values V#1, V#2 and V#n, respectively. In some embodiments as illustrated in FIG 4, in order to obtain variable discrete frequency dependent gain, several equalization circuits are cascaded to provide a discrete set of gain values.

[0055] The discrete gain values V#1, V#2, ..., V#n are fed to inputs of the multiplexer 416. Control logic input to multiplexer 416 is used as a select input to multiplexer 416 to select an appropriate one of the discrete gain values. This selection and control may be based on, for example, required equalizer transfer characteristics, for example. In some embodiments the control logic selects the appropriate number of output stages for the required equalizer transfer characteristics.

[0056] In some embodiments equalization circuits 404, 406 and 408 are different by varying resistance and capacitance values in the different circuits. For example, in some embodiments in which each of the equalization circuits 404, 406, ..., 408 are equalization circuits 300, each of those equalization circuits have different resistance values R2 of resistor 312 and different capacitance values C1 of capacitor 314. In some embodiments different resistance and capacitance values are chosen based on interconnect length.

[0057] FIG 5 is a waveform representation of a frequency response 500. Frequency response 500 may be a frequency response for the discrete gain values V#1, V#2, ..., V#n provided by apparatus 400 illustrated in FIG 4, for example. Waveforms 500 include a gain signal 502 (V#1), a gain signal 504 (V#2) and a gain signal 506 (V#n). As evident from FIG 5, by enabling a number of equalization stages (for example, using the cascaded equalization circuits of FIG 4) the frequency dependent transfer function can be varied in discrete steps.

[0058] FIG 6 illustrates an apparatus 600 according to some embodiments. In some embodiments apparatus 600 may be referred to as a DC feedback loop. In some

embodiments apparatus 600 may be referred to as a control circuit. In some embodiments the DC feedback loop 600 is used to adaptively equalize. In some embodiments the adaptive equalization may be used at a receiver to equalize frequency dependent loss over a transmission line or interconnect. In some embodiments apparatus 600 may be a feedback loop based on 8B/10B encoded signal characteristics of DC balance. In some embodiments apparatus 600 is used to select the output of a multiplexer and enable a required number of equalization stages based on a loss (for example, an interconnect loss).

[0059] Apparatus 600 includes a DC reference voltage value 602, an average DC voltage detector 604, a comparator 606, control logic 608 and a multiplexer 610. The multiplexer 610 may be the same multiplexer 416 as illustrated in FIG 4 or a different multiplexer. Additionally, DC reference 602, average DC detector 604, comparator 606 and control logic 608 may be used in the some embodiments illustrated in FIG 4 by plugging those elements in where the "control" input to multiplexer 416 is illustrated in FIG 4. Similarly, the elements of the gain circuit and/or the apparatus 400 of FIG 4 may be plugged in to the apparatus illustrated in FIG 6. In some embodiments the gain circuit illustrated in FIG 4 provides the discrete gain values V#1, V#2, ..., V#n illustrated in FIG 6.

[0060] Average DC detector 604 detects a DC voltage content of the output signal Out from multiplexer 610. Comparator 606 compares the detected DC content from average DC detector 604 with the DC reference value 602. In some embodiments DC reference 602, average DC detector 604 and comparator 606 figure out and compare the DC content of the output using a DC balance arrangement. Control logic 608 is used to select one of the discrete gain values V#1, V#2, ..., V#n. Control logic 608 is programmed, for example, by providing more attenuation at high frequency and less attenuation at low frequency.

[0061] FIG 7 illustrates an apparatus 700 according to some embodiments. In some embodiments apparatus 700 is an equalization circuit. Apparatus 700 includes an amplifier 702, a gain circuit 704 and a control circuit 706.

[0062] Amplifier 702 has an input IN and an inverse input $\overline{IN}$ and an output. The output of the amplifier 702 is provided as an input to gain circuit 704. Gain circuit 704 provides two or more discrete gain values V#1, V#2, ..., V#n. In some embodiments gain circuit 704 is the gain circuit illustrated in FIG 4 that provides discrete gain values V#1, V#2,....., V#n. Discrete gain values V#1, V#2, ..., V#n illustrated in FIG 7 can be the same as or different than discrete gain values V#1, V#2, ..., V#n illustrated in FIG 4. Control circuit 706 receives the two or more discrete gain values V#1, V#2, ..., V#n and provides an output Out in response to the discrete gain values. In some embodiments control circuit 706 selects one of the discrete gain values V#1, V#2, ..., V#n as the output Out. In some embodiments control circuit 706 is implemented using the apparatus 600 illustrated in FIG 6 (for example, control circuit or feedback loop, etc.). In some embodiments gain circuit 704 and control circuit 706 adaptively equalize the output from amplifier 702.

[0063] FIG 8 illustrates a system 800 according to some embodiments. System 800 includes a transmitter 802, a receiver 804 and a transmission line (or interconnect) 806. Receiver 804 includes an equalization circuit 812. In some embodiments equalization circuit 812 adaptively equalizes a loss in a signal. The equalization may necessary, for example, due to a loss on the transmission line (or interconnect) 806, or some other loss. In some embodiments equalization circuit 812 is an equalization circuit similar to or the same as equalization circuit 700 illustrated in FIG 7.

[0064] In some embodiments illustrated and described herein a single ended signaling scheme is used. However, some embodiments are implemented in a scheme using differential signals.

In some embodiments equalization is performed in chip-to-chip communication using high speed serial point-to-point interconnects.

[0065] In each system shown in a figure, the elements in some cases may each have a same reference number or a different reference number to suggest that the elements represented could be different and/or similar. However, an element may be flexible enough to have different implementations and work with some or all of the systems shown or described herein. The various elements shown in the figures may be the same or different. Which one is referred to as a first element and which is called a second element is arbitrary.

[0066] An embodiment is an implementation or example of the inventions. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the inventions. The various appearances "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.

[0067] If the specification states a component, feature, structure, or characteristic "may", "might", "can" or "could" be included, for example, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0068] Although flow diagrams may have been used herein to describe embodiments, the inventions are not limited to those diagrams or to corresponding descriptions herein. For example, flow need not move through each illustrated box or exactly in the same order as illustrated and described herein.

[0069] The inventions are not restricted to the particular details listed herein. Indeed, those skilled in the art having the benefit of this disclosure will appreciate that many other variations from the foregoing description and drawings may be made within the scope of the present inventions. Accordingly, it is the following claims including any amendments thereto that define the scope of the inventions.